IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (currently amended) A circuit for jitter measurement, comprising:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal, the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage ~~element~~ elements [[any]] one or more [[pulse]] pulses that [[is]] may be active at the time of occurrence of the trigger signal, wherein the second set of circuitry further includes a single one detector operative to select one from the recorded pulses in the storage elements at the time of occurrence of the trigger signal, and wherein a jitter measurement is made based on the selected pulses [[recorded in the storage elements]] after a plurality of trigger signals has occurred.

2. (previously presented) The circuit of claim 1, wherein the output of one delay element is connected to the input of the next adjacent delay element.

3. (previously presented) The circuit of claim 1, wherein the number of delay elements in the chain is N, where N is an even number greater than 2 and implemented as a

power of 2.

4. (previously presented) The circuit of claim 1, wherein the associated delay of each delay element is controlled by a delay control circuit.

5. (previously presented) The circuit of claim 4, wherein at least one of the plurality of associated delays is not equal to any other of the plurality of associated delays, and wherein the delay control circuit is a charge pump controlled delay lock loop.

6. (previously presented) The circuit of claim 1, wherein the first set of circuitry includes a plurality of two-input logic gates with each of the plurality of two-input logic gates corresponding to a respective one of the plurality of delay elements.

7. (previously presented) The circuit of claim 6, wherein each of the plurality of two-input logic gates is coupled to the input and the output of a corresponding one of the plurality of delay elements.

8. (previously presented) The circuit of claim 7, wherein one of the two inputs of each two-input logic gate is coupled to the output of its corresponding delay element via an inverter logic gate.

9. (currently amended) The circuit of claim 7, wherein one of the two inputs of each ~~of~~ two-input logic gate is coupled to the output of its corresponding delay element by means of wired connection.

10. (previously presented) The circuit of claim 6, wherein each of the plurality of two-input logic gates is capable of producing a pulse with a width approximately equal to the delay of its corresponding delay element.

11. (previously presented) The circuit of claim 1, wherein the second set of circuitry includes a first plurality of latching circuits each corresponding to one of the plurality

of delay elements.

12. (previously presented) The circuit of claim 1, wherein the input clock signal is related to a reference clock signal.

13. (previously presented) The circuit of claim 12, wherein the trigger signal is delayed by a first predetermined delay from the reference clock signal.

14. Cancelled.

15. (previously presented) The circuit of claim 13, wherein a measure of jitter is determined by comparing a latched pulse to the first predetermined delay.

16. Cancelled.

17. Cancelled.

18. (previously presented) The circuit of claim 1, wherein pulses are recorded for a first number of significant instants of the trigger signal.

19. (previously presented) The circuit of claim 1, further comprising a third set of circuitry for recording pulses.

20. (previously presented) The circuit of claim 19, wherein the third set of circuitry includes a second plurality of latching circuits each corresponding to one of the plurality of delay elements.

21. (previously presented) The circuit of claim 20, wherein each of the second plurality of latching circuits is provided with logic circuitry in a feedback loop for recording the presence of a desired input to the second plurality of latching circuits.

22. (previously presented) The circuit of claim 21, wherein the desired input to the second plurality of latching circuits is a logic level high.

23. (previously presented) The circuit of claim 1, further comprising a result calculator configured to provide information collected from the measure of jitter.

24. (currently amended) The circuit of claim [[19]]20, further comprising a result calculator connected to the second plurality of latching circuits and configured for receiving recorded pulses and based thereon providing information on an earliest occurrence in the chain of the significant instant of the propagating input clock signal.

25. (currently amended) The circuit of claim [[19]]20, further comprising a result calculator connected to the second plurality of latching circuits and configured for receiving recorded pulses and based thereon providing information on a latest occurrence in the chain of the significant instant of the propagating input clock signal.

26. (currently amended) The circuit of claim [[19]]20, further comprising a result calculator connected to the second plurality of latching circuits and configured for receiving recorded pulses and based thereon providing information on a difference between an earliest and a latest occurrence in the chain of the significant instant of the propagating input clock signal.

27. (currently amended) The circuit of claim [[19]]20, further comprising a result calculator connected to the second plurality of latching circuits and configured for receiving recorded pulses and based thereon providing median or average information on the occurrences of the significant instant of the input clock signal.

28. Cancelled.

29. (currently amended) The circuit of claim [[19]]20, further comprising a result calculator connected to the second plurality of latching circuits and configured for

receiving recorded pulses and based thereon providing information on a standard deviation in the occurrences of the significant instant of the input clock signal.

30. (previously presented) The circuit of claim 23, wherein the result calculator is configured to provide information responsive to a mode selection signal.

31. (currently amended) A method for measuring jitter of a clock signal, comprising:

for each of a plurality of trigger signal occurrences, performing the steps of

receiving the clock signal, the clock signal having a significant instant;

propagating the significant instant of the clock signal through a chain of delay elements, wherein each element has an associated delay and the chain has a total delay equal to the sum of the associated delays;

receiving a trigger signal and delaying the received trigger signal to occur at a time equal to approximately half the total delay of the chain;

detecting propagation of the significant instant of the clock signal through each of the delay elements in the chain and producing a pulse corresponding thereto;

if multiple pulses are produced coincident with the trigger signal, filtering the multiple pulses to provide one filtered pulse coincident with the trigger signal;

recording [[any]] the filtered pulse that is coincident with the trigger signal; [[and]]

producing a jitter measurement signal responsive to the [[recorded]]filtered pulses after the plurality of trigger signal occurrences.

32. (previously presented) The method of claim 31, further comprising deriving a jitter measure through a comparison of the jitter measurement signal to an associated delay.

33. Cancelled.

34. (currently amended) The method of claim [[33]]31, wherein the filtered [[jitter measurement signal]] pulse contains information of an earliest occurrence in the chain

of the propagating significant instant of the input clock signal.

35. (currently amended) The method of claim [[33]]31, wherein the filtered [[jitter measurement signal]] pulse contains information of a latest occurrence in the chain of the propagating significant instant of the input clock signal.

36. Cancelled.

37. (currently amended) The method of claim [[36]]31, wherein the filtering step further [[comprising]] comprises determining an earliest occurrence in the chain of the propagating significant instant.

38. (currently amended) The method of claim [[36]]31, wherein the filtering step further [[comprising]] comprises determining a latest occurrence in the chain of the propagating significant instant.

39. (currently amended) The method of claim [[36]]31, wherein the filtering step further [[comprising]] comprises determining a difference between an earliest and latest occurrence in the chain of the propagating significant instant.

40. (currently amended) The method of claim [[36]]31, further comprising determining statistical information on the occurrences in the chain of the propagating significant instant.

41. (currently amended) The method of claim 31, wherein an associated frequency of the [[reference]] clock signal is adjusted in response to the jitter measurement signal.

42. (previously presented) The method of claim 31, wherein the trigger delay is adjusted in response to the jitter measurement signal.

43. (currently amended) The method of claim 31, further comprising receiving a reset

signal, wherein the [[resent]] reset signal is delayed by a second delay relative to the reference clock signal which is adjusted in accordance with the jitter measurement signal.

44. (previously presented) The method of claim 31, further comprising inputting the reference clock signal to a circuit to produce the input clock signal.

45. (previously presented) The method of claim 44, wherein the circuit is adjusted in accordance with the jitter measurement signal.

46. (previously presented) A system for responding to jitter therein, comprising:

a reference clock configured to generate a reference clock signal having an associated frequency;

a plurality of circuits configured to receive the reference clock signal and operative to generate an input clock signal, the plurality of circuits having a first set of characteristics; and

a jitter measurement sub-system configured to receive the reference clock signal and the input clock signal and operative to generate a jitter measurement output signal responsive to a significant instant of the input clock signal, wherein the jitter measurement sub-system includes:

a plurality of delay elements having a plurality of associated delays configured to generate a synthesized signal from the reference clock signal and the input clock signal; and

at least one programmable delay element having at least one associated programmable delay configured to produce a trigger signal for generating the jitter measurement output signal from the synthesized signal;

wherein the system is operative to adjust at least one parameter of the system in accordance with the jitter measurement output signal.

47. (original) The system of claim 46, wherein the at least one parameter of the system is at least one parameter of the jitter measurement sub-system.

48. (original) The system of claim 46, wherein the at least one parameter includes the associated frequency.

49. (original) The system of claim 46, wherein the reference clock signal further has an associated duty cycle, and the at least one parameter includes the associated duty cycle.

50. (original) The system of claim 46, wherein the at least one parameter includes at least one characteristic from the first set of characteristics.

51. (previously presented) The system of claim 46, wherein the plurality of circuits includes a plurality of sub-circuits having a second set of characteristics, and wherein the at least one parameter includes at least one characteristic from the second set of characteristics.

52. (previously presented) The system of claim 46, wherein the output of one delay element is connected to the input of the next adjacent delay element.

53. (previously presented) The system of claim 46, wherein at least one of the plurality of associated delays is not equal to any other of the plurality of associated delays.

54. (original) The system of claim 46, wherein the at least one parameter includes at least one of the plurality of associated delays.

55. (original) The system of claim 46, wherein the at least one parameter includes all of the plurality of associated delays.

56. (original) The system of claim 46, wherein the at least one parameter includes the at least one associated programmable delay.

57. (currently amended) A jitter measurement circuit comprising:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to the sum of the delays of the delay elements, wherein the first element in the chain has an input that receives an input clock signal, the chain propagating the input clock signal through each of its elements, and each delay element output producing a delayed version of the signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay which is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage element any pulse that is active at the time of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality of trigger signals has occurred;

a single one detector for receiving a reset signal and for filtering the measure of jitter by selecting one instance of the recorded pulses in response to occurrence of the reset signal; and

a result calculator for producing statistical information about occurrences in the chain of the significant instance of the input clock signal.

58. Cancelled.